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SPI FLASH INTERFACE SPECIFICATION



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SPI Flash Interface Specification

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Notices and other considerations

Important notices

- Datakey Electronics, Inc., guarantees the quality of its portable memory devices by testing them before shipment. However, installing and using Datakey Electronics products is the responsibility of the purchaser and is in no way guaranteed by Datakey Electronics.
 - Timing data, electrical characteristics, and signal descriptions are based on a compilation of several approved manufacturer specifications. Datakey Electronics reviews the specifications of all approved vendors and "de-rates" the specifications as necessary to ensure that all devices meet our published specifications regardless of the vendor used.
 - Customers must design to our published specifications to ensure that all devices operate correctly within an application. Designing to a particular vendor's specification is not recommended.
 - While the information in this specification has been carefully reviewed, Datakey Electronics assumes no liability for any errors or omissions in this specification. Additionally, Datakey Electronics reserves the right to make changes to any part of the information in this specification or the products described herein without further notice.
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Other considerations

- Although portable memory devices are designed to withstand harsh environments, many of the conditions that prevent them from functioning properly in those environments are best addressed through the proper design of system interface circuits.
 - Datakey Electronics tests all Keys and Tokens during the manufacturing process. In some cases, data written to a memory device remains after the test. Users should not rely on this data as a means of identifying Keys or Tokens.
-

SPI Flash Interface Specification

Introduction

General description

Datakey Electronics portable memory Keys and Tokens contain programmable memory based on EEPROM or Flash technology. Access to these devices is through a serial bus interface, using the Microwire, I²C or Serial Peripheral Interface (SPI) bus protocols. Each protocol controls the device input and output pins through separate serial interface formats.

Portable memory device uses

Portable memory devices add functional versatility to many applications. They personalize equipment operations and transfer data in the following applications:

- Access control devices
 - Instrument calibration equipment
 - Fuel dispensers
 - Medical treatment systems
-

Memory device design criteria

Portable memory applications need memory devices that can survive outside traditional environments; they must maintain data integrity when you insert and remove them from their active hosts. Therefore, all portable memory devices must be able to meet the following basic design criteria:

- Resist dirt and other contaminants
 - Transfer data reliably
 - Tolerate electrostatic discharge
 - Retain data when power is removed
 - Retain data when exposed to certain environmental hazards
-

Manufacturers' design responsibility

Portable memory device manufacturers need to meet these basic design criteria because the devices must be capable of surviving in harsh environments. When integrating a memory device into a larger system, manufacturers need to consider the following:

- How to dissipate electrostatic discharge (ESD)
 - How to maintain device data integrity
 - How to prevent host system disruption when inserting and removing the Key or Token memory device
-

Continued on next page



Introduction, continued

**Datakey
Electronics
portable
memory devices**

Datakey Electronics designs and manufactures portable, rugged Keys and Tokens containing non-volatile memory. For more than 29 years, our tough, reliable, re-programmable Keys, Tokens, receptacles, and systems solve data transport and access control problems for the most extreme environments.

You can access SPI Flash Keys and Tokens containing serial Flash memory devices through a simple four-wire serial interface. Simple instructions control data transfers to and from the SPI Flash memory. This interface specification describes those instructions.

SPI Flash Key and Token data-integrity enhancements come through several means, including the Write Enable and Write Disable instructions. These instructions enable and disable the ability to overwrite data stored in the device. The correct use of these instructions reduces the potential for data corruption.

**This
specification**

The remaining pages in this specification discuss SPI Flash design criteria for portable memory devices and recommend ways to handle them in typical applications.

Functional description

Keys and Tokens

The following are examples of serial Flash devices available from Datakey Electronics. Each type of Key and Token shown below easily mates to a custom Keyceptacle®/Receptacle, providing access to its communication, power, and ground signals.



SFK or SFK5V



SFT



SFX

Signals

Table 1 shows the signals for the KC4210/KC4210PCB Keyceptacles and the SR4210/SR4210PCB Receptacles. Each Keyceptacle and Receptacle is described in the following pages.

Use the Keyceptacle to interface the SFK and SFK5V series Keys. Use the Receptacles to interface the SFT Tokens and SFX Extended Tokens.

Communication between the microcontroller and devices on an SPI bus uses four signals: an active-low Chip Select ($/CS$), a Serial Clock (SCK), a Serial Data In (SI) and a Serial Data Out (SO). In addition, an active low-hold ($/HOLD$) signal suspends communication with the Key or Token. Those signals, along with the voltage supply (V_{CC}) and ground signals, are present on all Keys and Tokens.

Table 1: Signal Acronyms and Descriptions

Signal Acronym	Signal Description
$/CS$	Chip Select Input (<i>active-low</i>)
SI	Serial Data Input
SO	Serial Data Output
SCK	Serial Clock
$/HOLD$	Hold Input (<i>active-low</i>)
V_{CC}	Supply Voltage
V_{SS}	Ground

Continued on next page



Functional description, continued

Chip Select (/CS) The Chip Select signal is an active-low input to the device. A low level selects the device and places it in the active-power mode. A high level deselects the device and forces standby mode unless an internal programming, erase or write-status register cycle is in progress. After completing the write cycle, the device enters standby mode.

Serial Data In (SI) The Serial Data In signal is an input to the device. The instruction, address and data bits serially transfer to the device. Data values latch in on the rising edge of the serial clock signal.

Serial Data Out (SO) The Serial Data Out signal is an output from the device. The SO signal and the Serial Clock signal enable synchronous data outputs. Data values shift out on the falling edge of the serial clock signal.

Serial Clock (SCK) The Serial Clock signal is an input to the device. The SCK synchronizes the communication between the master device and the memory chip. The instruction, address, and data bits present on the SI pin clock in on the rising edge of the SCK signal. Data bits on the SO pin shift out on the falling edge of the SCK signal.

Supply Voltage (V_{CC}) Two versions of SPI Flash Keys and Tokens are available based on user-supply voltage requirements. The SFK, SFT, and SFX Keys and Tokens operate with a 3.3Vdc nominal supply. The SFK5V and SFX5V Keys and Tokens operate with a 5.0Vdc nominal supply. **The Vcc signal must be controlled so that Keys and Tokens are not inserted into “live” Keyceptacles®/Receptacles. See section entitled “Memory Device Power and Signal Control”.**

Ground (V_{SS}) The Ground signal and the System Ground signal are common.

Operating features

Operating features and device capacity

Datakey Electronics SPI Flash memory products share operating features that differ based on the capacity of the memory device. Each device offers features such as the following:

- Page programming
 - Sector and bulk erasing
 - Ability to monitor programming or erase cycles
 - Ability to write-protect portions of the memory space through software instructions
-

Memory device addressing

You can write data to the addressable memory locations of the memory device by issuing a Write Enable instruction followed by the Page Programming instruction. All SPI Flash memory products are organized in pages of 256 bytes. Programming one byte of data within a 256-byte page achieves the programming of all bytes on that page. Therefore, the Page Programming instruction enables the downloading of up to 256 bytes in the same instruction. That capability reduces the overhead for writing data to the memory device.

Sector and chip erase

Writing data to the memory device involves changing the state of memory bits from “1” to “0.” You cannot program a bit from “0” to “1.” SPI Flash memory devices do not include an automatic erase cycle before a write cycle. Therefore, you can erase individual sectors or the entire device with the Sector Erase or Chip Erase instruction. The size of an individual sector and the number of sectors within a device varies with the total capacity of the memory device. Information about the size and number of sectors for each SPI Flash memory type will be discussed later.

To reduce the risk of accidentally erasing the memory, a Write Enable instruction must be sent before issuing the Erase instruction.

Continued on next page

Operating features, continued

Status register The status register contains several status bits. These bits are read or set by specific instructions. Figure 1 shows the status register bit configurations.

The write-in-progress (WIP) bit: The WIP bit shows the status of the programming or erase cycle. When the write or erase cycle is in progress, the WIP bit has a value of “1.” After completing the write or erase cycle, the bit will be set to “0.”

The write-enable-latch (WEL) bit: The Write Enable or Write Disable instruction sets or resets the WEL bit. Before initiating a write or erase instruction, set the WEL bit, otherwise the instruction will be ignored. When powering up the device, or on the completion of a write or erase cycle, the WEL bit will be automatically reset to “0.”

BP2, BP1, and BP0 block-protect bits: The block-protect (BP) bits can be written with the Write Status Register instruction. Setting or resetting the BP bits determines which sectors within the addressable memory space will be write protected. The number of BP bits and memory sectors varies with memory device capacities.

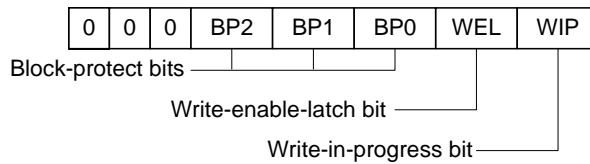


Figure 1: Status Register Bit Configurations

Continued on next page

Operating features, continued

Write protection You can write protect all or part of the addressable memory in all Keys and Tokens. The write protected area is based on the value written to the BP bits using the Write Status Register instruction. Memory locations inside protected sectors become read-only memory. Table 2 shows the protected sectors for each memory size, and the BP bit settings.

Table 2: Memory Size and Block-Protect Bit Settings

Block-protect (BP) bits			SFK 1M, SFT 1M SFK5V 1M	SFK 2M, SFT 2M SFK5V 2M	SFK 4M, SFT 4M SFK5V 4M	SFK 8M, SFT 8M SFK5V 8M
<i>BP2</i>	<i>BP1</i>	<i>BP0</i>	<i>Protected Sectors</i>	<i>Protected Sectors</i>	<i>Protected Sectors</i>	<i>Protected Sectors</i>
0	0	0	None	None	None	None
0	0	1	3	3	7	15
0	1	0	2 and 3	2 and 3	6 and 7	14 and 15
0	1	1	All	All	4 to 7	12 to 15
1	0	0			All	8 to 15
1	0	1			All	All
1	1	0			All	All
1	1	1			All	All

The 1M and 2M memory sizes do not have a BP2 bit position. This bit-position value should be “0” when data passes with the Write Status Register instruction.

All Page Programming and Erase instructions that affect memory addresses within a protected sector will be ignored.

NOTE: For memory sizes greater than 8Mbits review Addendum A, page 47.

Continued on next page

Operating features, continued

/Hold signal All SPI Flash memory Keys and Tokens provide access to the /Hold signal. It can interrupt communications with the device without terminating the data output or the instruction. You can use this feature when a higher priority device on the same SPI bus interrupts the controller.

Hold condition Normally, a Hold condition starts when the /Hold signal goes low while the Serial Clock (SCK) signal is low. In this case, the Hold condition will start immediately. During a Hold condition, the Serial Data Out (SO) pin will be in a high impedance state, and signals on the SCK and the Serial Data In (SI) pins will be ignored. If the SCK signal is low when the /Hold signal goes high, the Hold condition will end immediately.

If you apply or remove the /Hold signal while the serial clock signal is high, the Hold condition will not start or end until the next falling edge of the SCK signal.

The Hold condition is only effective at suspending communications with the memory device while the device remains selected by the /CS signal. If you deselect the device by removing the low level on the /CS signal during a Hold condition, the internal logic of the device will reset. In this case, reselect the device with a /CS signal. Resend the interrupted instruction once the /Hold signal goes high.

Figure 2 shows standard and non-standard application /Hold signal timing.

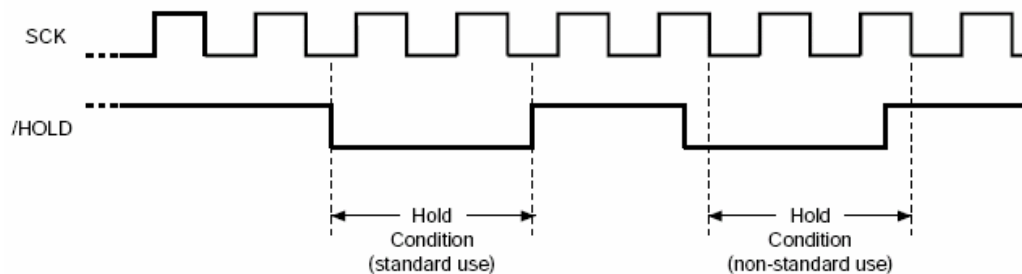


Figure 2: Standard and Non-Standard Application /Hold Signal Timing

Instructions

Common instruction set

All Datakey Electronics SPI Flash memory products operate with the following set of common instructions:

- Basic instructions to read and write from any addressable memory location
 - Instructions to erase all or a portion of the memory area
 - Instructions to write-protect areas of memory
 - Instructions to read the size of the memory device embedded in a Key or Token
-

Device data transfers

All instructions, addresses, and data shift into the device on the Serial Data In (SI) signal. Data shifts out of the device on the Serial Data Out (SO) signal. All serial data shifts in or out, beginning with the most significant bit.

Unless you select the device by driving the /CS signal low, serial data on the SI signal will be ignored. Serial data latches into the key or token on the rising edge of the SCK signal. Each instruction sequence begins with an instruction byte followed by an address or data, depending on the instruction.

For instructions that require data from the device, such as Read or Read Status instructions, the data shifts out beginning with the most significant bit immediately following the instruction and the data in sequence. Data shifts out on the falling edge of the SCK signal.

Continued on next page

Instruction set descriptions Table 3 lists the instruction set common to all SPI Flash Keys and Tokens. It is possible to follow instruction bits with additional information such as address and data, depending on the type of instruction. Each instruction will be described in detail later.

Table 3: Common Instruction Set for SPI Flash Keys and Tokens

Instruction	Description	Instruction Bits	Address Bytes	Extra Bytes	Data Bytes
WREN	Write Enable	00000110b (06h)	0	0	0
WRDI	Write Disable	00000100b (04h)	0	0	0
RDSR	Read Status Register	00000101b (05h)	0	0	1 - ∞
WRSR	Write Status Register	00000001b (01h)	0	0	1
READ	Read Data	00000011b (03h)	3	0	1 - ∞
FAST_READ	Read Data at higher speed	00001011b (0Bh)	3	1	1 - ∞
PP	Page Program (<i>write data</i>)	00000010b (02h)	3	0	1 - 256
SE	Sector Erase	11011000b (D8h)	3	0	0
BE	Bulk or Chip Erase	11000111b (C7h)	0	0	0
DP	Deep Power-down	10111001b (B9h)	0	0	0
RES	Release from Power-down and Read Electronic Signature	10101011b (ABh)	0	3	1 - ∞

SPI Flash Key and Token memory capacities SPI Flash Keys and Tokens have different memory capacities based on the device type. The addressable memory range is based on the memory capacity. SPI Flash Keys and Tokens are available in memory capacities of 1, 2, 4 or 8 megabits. The memory space arrangement is byte-wide memory locations organized in 256 byte pages. Additionally, each device is divided into several sectors of 32,768 bytes or 65,536 bytes, depending on the device type.

Table 4 shows the total device size, the number of pages, the size and address range of each sector, and the number of sectors for each Key and Token type.

NOTE: For memory sizes greater than 8Mbits review Addendum A, page 47.

Continued on next page

Instructions, continued

Table 4: Key and Token Capacities and Sector Address Ranges

	SFK 1M SFT 1M SFK5V 1M	SFK 2M SFT 2M SFK5V 2M	SFK 4M SFT 4M SFK5V 4M	SFK 8M SFT 8M SFK5V 8M
Device Signature	10h	11h	12h	13h
Device Size (Bytes)	131072	262144	524288	1048576
Pages	512	1024	2048	4096
Page Size (Bytes)	256	256	256	256
Sectors	4	4	8	16
Sector Size (Bytes)	32768	65536	65536	65536
Sector Address Range				
0	00000h to 07FFFh	00000h to 0FFFFh	00000h to 0FFFFh	00000h to 0FFFFh
1	08000h to 0FFFFh	10000h to 1FFFFh	10000h to 1FFFFh	10000h to 1FFFFh
2	10000h to 17FFFh	20000h to 2FFFFh	20000h to 2FFFFh	20000h to 2FFFFh
3	18000h to 1FFFFh	30000h to 3FFFFh	30000h to 3FFFFh	30000h to 3FFFFh
4			40000h to 4FFFFh	40000h to 4FFFFh
5			50000h to 5FFFFh	50000h to 5FFFFh
6			60000h to 6FFFFh	60000h to 6FFFFh
7			70000h to 7FFFFh	70000h to 7FFFFh
8				80000h to 8FFFFh
9				90000h to 9FFFFh
10				A0000h to AFFFFh
11				B0000h to BFFFFh
12				C0000h to CFFFFh
13				D0000h to DFFFFh
14				E0000h to EFFFFh
15				F0000h to FFFFFh

Continued on next page

**Memory
addresses**

You can read data from or write data to any memory location within the address range of the device. Three address bytes or 24 address bits following the Read or Write instruction specify the address location. You can read data beginning with any permissible address. Once data from an address shifts out, the internal address pointer automatically increments, and then you can read data from the next location. In this manner, one Read instruction reads the entire contents of the device.

You can write to any address location by specifying the address in the Write instruction. Consecutive locations may be written by sending up to 256 bytes of data. During a write operation, the internal address pointer will increment automatically until it reaches the page boundary. At that point, the address will reset to the beginning of the current page. Therefore, it is possible to overwrite previously written data.

**Sector or
Device Erase
instruction**

SPI Flash memory devices do not have automatic erase cycles while writing data to the memory. Issue a Sector or Bulk Erase instruction before writing data. It is important to note that data is written in pages of 256 bytes, but data is erased as sectors containing 32,768 or 65,536 bytes depending on the memory size.

IMPORTANT

All Keys and Tokens are tested during the manufacturing process. In some cases, the testing process leaves test data or artifacts on the Key or Token. Users must erase Keys or Tokens before using them.

Instruction descriptions

Write Enable instruction

Issue a Write Enable (WREN) instruction before each type of write operation, including the Page Program (PP), Sector Erase (SE), Bulk Erase (BE), and Write Status Register (WRSR) instructions. The Write Enable instruction sets the write-enable-latch (WEL) bit in the status register.

Execute the Write Enable instruction by selecting the device with a low level on the /CS signal—transmitting the instruction on the SI signal and deselecting the device. Figure 3 shows the WREN instruction timing sequence.

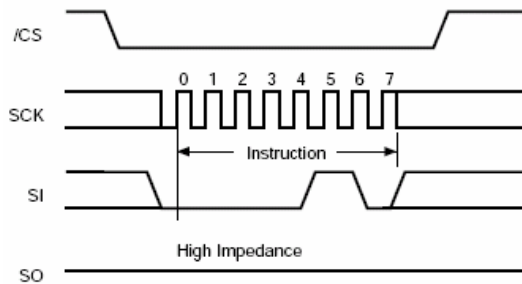


Figure 3: WREN Instruction Timing Sequence

Write Disable instruction

A Write Disable (WRDI) instruction resets the WEL bit in the status register, which prevents writing or erasing data. Execute the Write Disable instruction by selecting the device with a low level on the /CS signal—transmitting the instruction on the SI signal and deselecting the device. Figure 4 shows the WRDI instruction timing sequence.

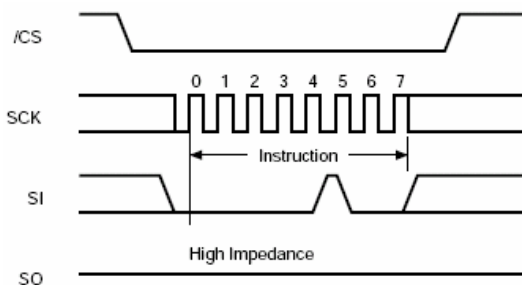


Figure 4: WRDI Instruction Timing Sequence

Note: The WEL bit will reset automatically when the device powers up or upon the completion of an instruction to program or erase the memory.

Continued on next page

Instruction descriptions, continued

Status register bit definitions

The number of block-protect (BP) bits is dictated by the memory capacity of the Key or Token. A description of these bits is in the operating features section of this document.

The write-enable-latch (WEL) bit is set to “1” with a Write Enable instruction. When the WEL bit is set to “1,” the Write or Erase instruction will be effective. The WEL bit will set automatically to “0” when completing any Write or Erase instruction. It will also be set to “0” when the device powers up or when executing a Write Disable instruction.

The write-in-progress (WIP) bit shows when the memory is busy with a write or erase operation. When the write or erase cycle is in progress, the bit is set to “1.” After completing the write or erase cycle, the bit is set to “0.”

Write Status Register (WRSR) instruction

The Write Status Register instruction sets the value of the BP bits. All other bits in the status register are read-only bits, with the exception of the WEL bit. The WEL bit is set or reset with the WREN and WRDI instructions respectively.

Send the Write Enable instruction before the Write Status Register instruction. Execute the Write Status Register instruction by selecting the device with a low level on the /CS signal—transmitting the instruction followed by the data on the SI signal, and deselecting the device. Figure 7 shows the WRSR instruction timing sequence.

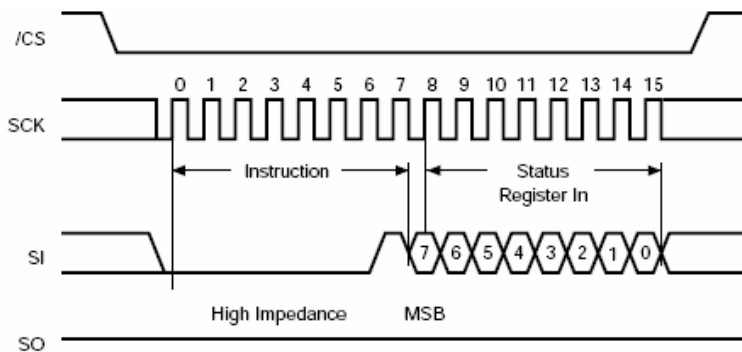


Figure 7: The WRSR Instruction Timing Sequence

Note: Only the appropriate block protect bits are effective (*bit positions B2, B1, and B0*). See Figure 6. Set all other data bits to a value of “0.” The size of the memory device determines the number of BP bits.

Continued on next page

Instruction descriptions, continued

Read Data Bytes (READ) instruction

The READ instruction enables reading memory locations within the addressable range of the device. Execute the READ instruction by selecting the device with a low level on the /CS signal—transmitting the instruction on the SI signal, followed by the 24-bit address. The contents of the addressed memory location shift out on the SO signal, on the falling edge of the SCK signal. Figure 8 shows the READ instruction timing sequence.

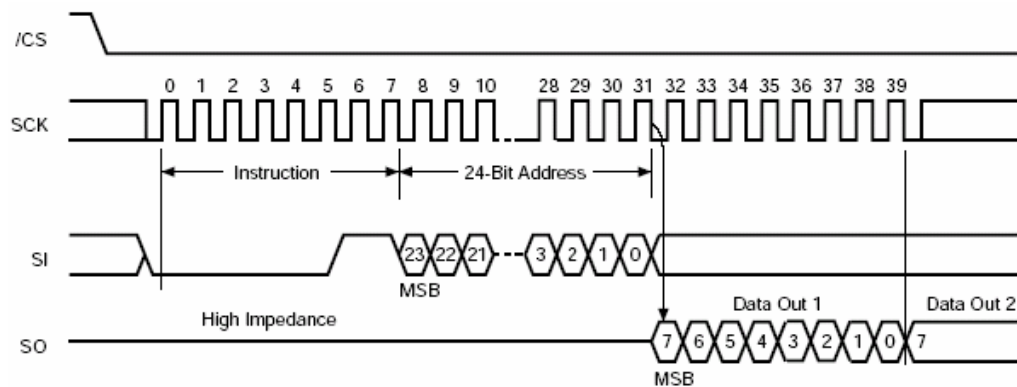


Figure 8: READ Instruction Timing Sequence

READ instruction memory addressing

The maximum clock frequency for the READ instruction is specified as f_{SCKR} . The internal address pointer will increment automatically after outputting a byte of data. Data from the next memory address shifts out on the SO signal as long as there is an SCK signal and the /CS signal remains low. The internal memory address rolls over to location “0” when data from the highest addressable memory location shifts out. To terminate the READ instruction, deselect the device with a high level on the /CS signal.

Note: The address bits that reference memory locations beyond the addressable range of the device are ignored.

Continued on next page

Instruction descriptions, continued

Fast Read Data Bytes (FAST_READ) instruction

The FAST_READ instruction performs the same function as the Read Data Bytes (READ) instruction except that it allows the data to shift out at a higher frequency. Execute the FAST_READ instruction by selecting the device with a low level on the /CS signal—transmitting the instruction, the 24-bit address, and a dummy byte on the SI signal. The contents of the addressed memory location shift out on the SO signal, on the falling edge of the SCK signal. Figure 9 shows the FAST_READ instruction timing sequence.

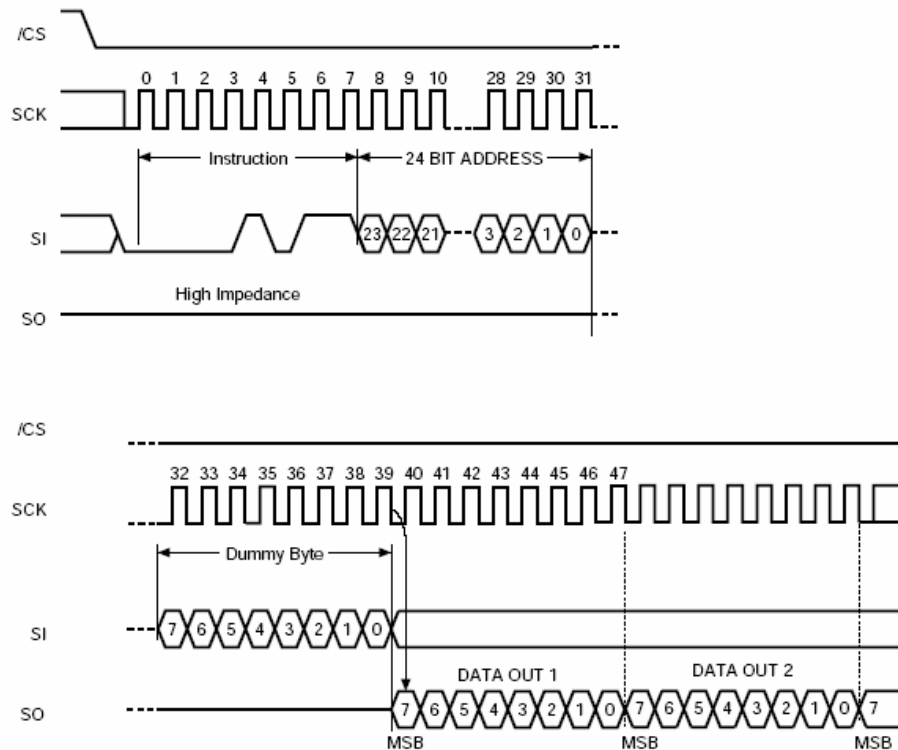


Figure 9: FAST_READ Instruction Timing Sequences

Continued on next page

Instruction descriptions, continued

Fast_Read instruction memory addressing

The maximum clock frequency for the FAST_READ instruction is specified as f_{SCK} . The internal memory address automatically increments after outputting each data byte. Data from the next memory location shifts out on the SO signal as long as there is an SCK signal and the /CS signal remains low. The internal memory address rolls over to location “0” when the data from the highest addressable memory location shifts out. To terminate the FAST_READ instruction, deselect the device with a high level on the /CS signal.

Note: The address bits that reference memory locations beyond the addressable range of the device are ignored.

Programming memory locations

The Write Data Bytes/Page Program (PP) instruction programs memory locations with data. Erase the memory locations before programming them because the PP instruction can only change bit states from “1” to “0.” Before sending a PP instruction, execute a Write Enable (WREN) instruction to set the write-enable-latch bit in the status register.

Page Program (PP) instruction

Execute the Page Program instruction by selecting the device with a low level on the /CS signal—transmitting the instruction on the SI signal, followed by the desired 24-bit address and at least one data byte. You can transmit additional data bytes if they reside within the same 256-byte page selection of the address bits.

To terminate the instruction, deselect the device with a high level on the /CS signal. The /CS signal must go high only after latching the last bit of a data byte to prevent the entire Page Program instruction from being ignored. Figure 10 shows the PP instruction timing sequence.

Continued on next page

Instruction descriptions, continued

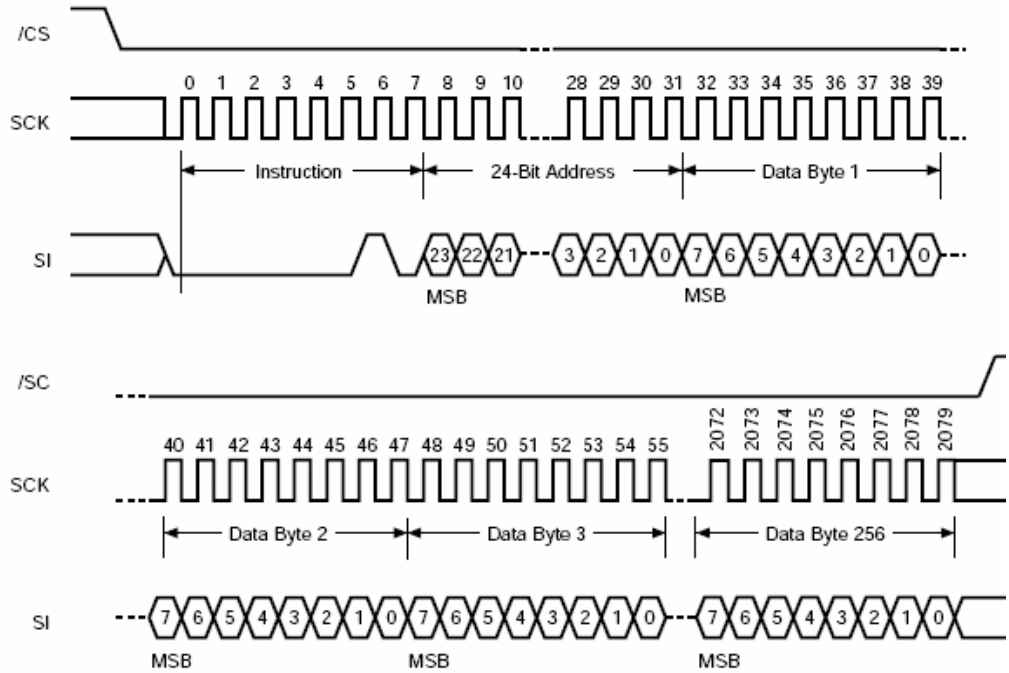


Figure 10: PP Instruction Timing Sequence

Programming pages

The PP instruction programs an entire 256-byte page; however, it is not necessary to transmit 256 bytes in the same instruction. All data transmissions within the instruction will be programmed within the same page. If the beginning address transmitted with the PP instruction points to a location not at the beginning of a page (*address bits A7 – A0 equal “0”*), then the address pointer will roll over to the beginning of the current page if the address exceeds the page boundary. Similarly, if you transmit more than 256 bytes of data with the PP instruction, the current data will be overwritten before programming the page.

Continued on next page

Instruction descriptions, continued

Self-timed page programming cycle The self-timed page programming cycle begins when the /CS signal is driven high. The page programming cycle time specifies the maximum duration of the page programming cycle. During this cycle, you can read the status register with the read Status Register (RDSR) instruction to monitor the write-in-progress (WIP) bit. The WIP bit will have a value of “1” during a programming cycle. After completing the programming cycle, the WIP bit and the write-enable-latch (WEL) bit will be set to “0.” A Page Program instruction will have no effect on pages within a protected block.

Sector Erase (SE) instruction The Sector Erase instruction sets all bits within the addressed sector to a value of “1.” Use the SE instruction to erase the memory locations within a sector (FFh) before writing data. To be effective, precede the SE instruction with a Write Enable instruction.

SE instruction timing Execute the SE instruction by selecting the device with a low level on the /CS signal—transmitting the instruction on the SI signal, followed by a 24-bit address that addresses a location within the sector. The self-timed erase cycle begins when the /CS signal is driven high after clocking in the last bit of the last address byte.

Figure 11 shows the SE instruction timing sequence. Table 4 on page 13 shows the range of addresses within sectors for all memory device sizes.

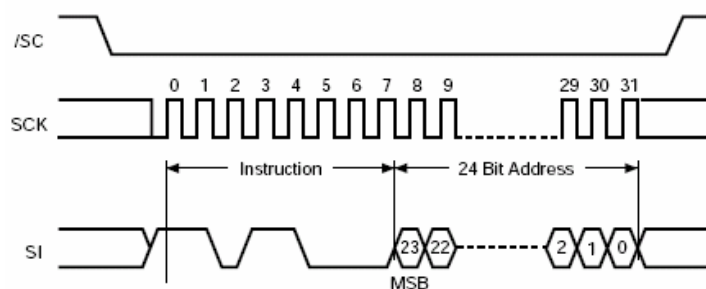


Figure 11: SE Instruction Timing Sequence

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Instruction descriptions, continued

Sector erase cycle duration

The maximum duration of the sector erase cycle is specified by t_{SE} . During this cycle, you can read the status register with the Read Status Register (RDSR) instruction to monitor the WIP bit. The WIP bit will have a value of “1” during an erase cycle. After completing the erase cycle, the WIP bit and the WEL bit will be set to “0.”

The SE instruction will have no effect on sectors within protected blocks.

Chip or Bulk Erase (CE) instruction

The Chip Erase instruction sets all bits in the entire memory to a value of “1.” To be effective, precede the CE instruction with a Write Enable instruction. Execute the CE instruction by selecting the device with a low level on the /CS signal—transmitting the instruction on the SI signal and deselecting the device. Figure 12 shows the Chip or Bulk Erase instruction timing sequence.

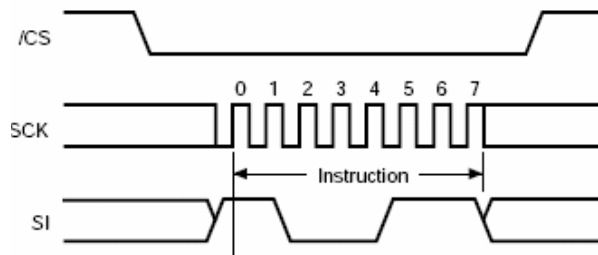


Figure 12: CE Instruction Timing Sequence

Chip or bulk erase cycle duration

The maximum duration of the chip or bulk erase cycle is specified by t_{BE} . This value depends on the size of the memory device. During the chip erase cycle, you can read the status register with the RDSR instruction to monitor the WIP bit. The WIP bit will have a value of “1” during a programming cycle. After completing the programming cycle, the WIP bit and the WEL bit will be set to “0.”

If one or more BP bits are set, the CE instruction will be ignored.

Continued on next page

Instruction descriptions, continued

Deep Power-Down (DP) instruction

The DP instruction places the device in the lowest current consumption mode possible without fully removing the power. This mode can be used to further protect memory from inadvertent write or erase conditions since all instructions except a Release from DP/Read Electronic Signature (RES) instruction will be ignored. Execute the DP instruction by selecting the device with a low level on the /CS signal—transmitting the instruction on the SI signal, and deselecting the device. The /CS high to power-down mode (t_{DP}) determines when the device will enter deep power-down mode.

Figure 13 shows the DP instruction timing sequence.

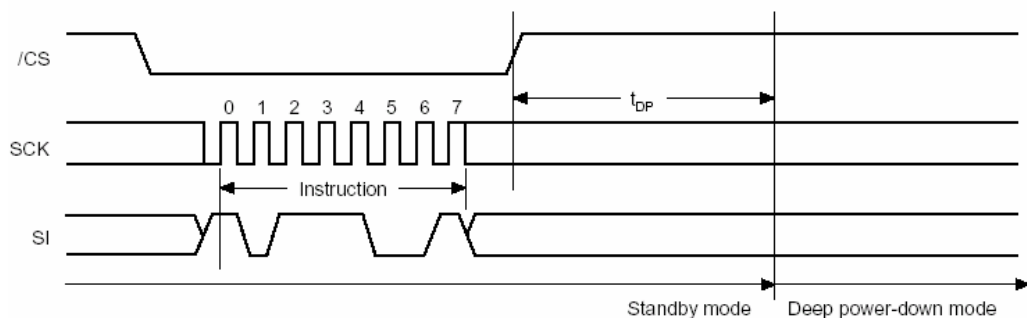


Figure 13: DP Instruction Timing Sequence

Deep power-down mode cancellation

Cycling power to the device will cancel deep power-down mode. The memory device always powers up in standby mode. The DP instruction will be ignored if transmitted during an erase or programming cycle.

Read Electronic Signature (RES)

In the deep power-down mode, the memory device will only recognize the Release from DP/Read Electronic Signature (RES) instruction. The RES instruction will place the device in standby mode. You can also issue a RES instruction while the device is active to read the electronic signature of the device.

Continued on next page

Instruction descriptions, continued

RES instruction Execute the RES instruction by selecting the device with a low level on the /CS signal—transmitting the instruction and three dummy bytes on the SI signal. The single byte electronic signature of the device shifts out on the SO pin with the falling edge of the SCK, following the last bit of the third dummy byte. After reading the electronic signature at least once, you can terminate the RES instruction by deselecting the device with a high level on the /CS signal. Output of the electronic signature byte will be repeated as long as the device remains selected and an SCK signal is provided.

Figure 14 shows the RES instruction timing sequence.

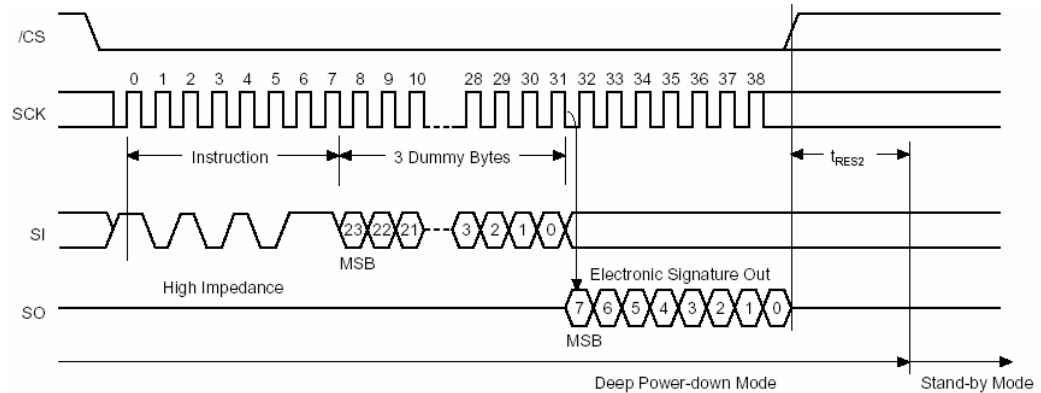


Figure 14: RES Instruction Timing Sequence

RES instruction and memory size The electronic signature is unique for each memory device size. The RES instruction is a convenient method of determining the size of the memory device being selected. See Table 4 on page 13 for a list of electronic signature bytes based on memory size.

If you transmit the RES instruction during a Programming or Erase instruction, the RES instruction will be ignored.

Panel- and board-mount Keyceptacle®/Receptacle descriptions

Keyceptacles/ Receptacles

The Keyceptacles/Receptacles are used to interface the host system directly with specific serial data Keys and Tokens. The styles are the KC4210, KC4210PCB, SR4210, and the SR4210PCB.

A Last On/First Off (LOFO) switch in the Key or Token Keyceptacle/Receptacle enables the host system to determine when a Key or Token is present. Upon insertion of a Key or Token, the LOFO contact connects to ground. Conversely, when the Key is removed, the LOFO contact is open. The LOFO contact allows system designers to detect the presence of a Key or Token and protect the host bus by only applying power after the device has been fully inserted into the host.

KC4210 panel- mount Keyceptacle

The KC4210 panel-mount version is designed for applications that require easy mounting in a front panel configuration. Figure 15 shows the panel-mount KC4210 Keyceptacle.

To mount the device, simply cut a one-inch square hole in the desired panel location and snap the Keyceptacle into place. Use a standard 10-pin connector cable (*5 x 2 pin configuration*) to connect the device to the host.



Figure 15: Panel-Mount KC4210 Keyceptacle

Note: Do not allow the total length of the signal conductors for PC board traces and ribbon cables to exceed eight inches.

Continued on next page

Panel- and board-mount Keyceptacle®/Receptacle descriptions, continued

KC4210 orthographic drawing

Figure 16 shows the KC4210 panel-mount Keyceptacle. Refer to spec sheet for dimensions.

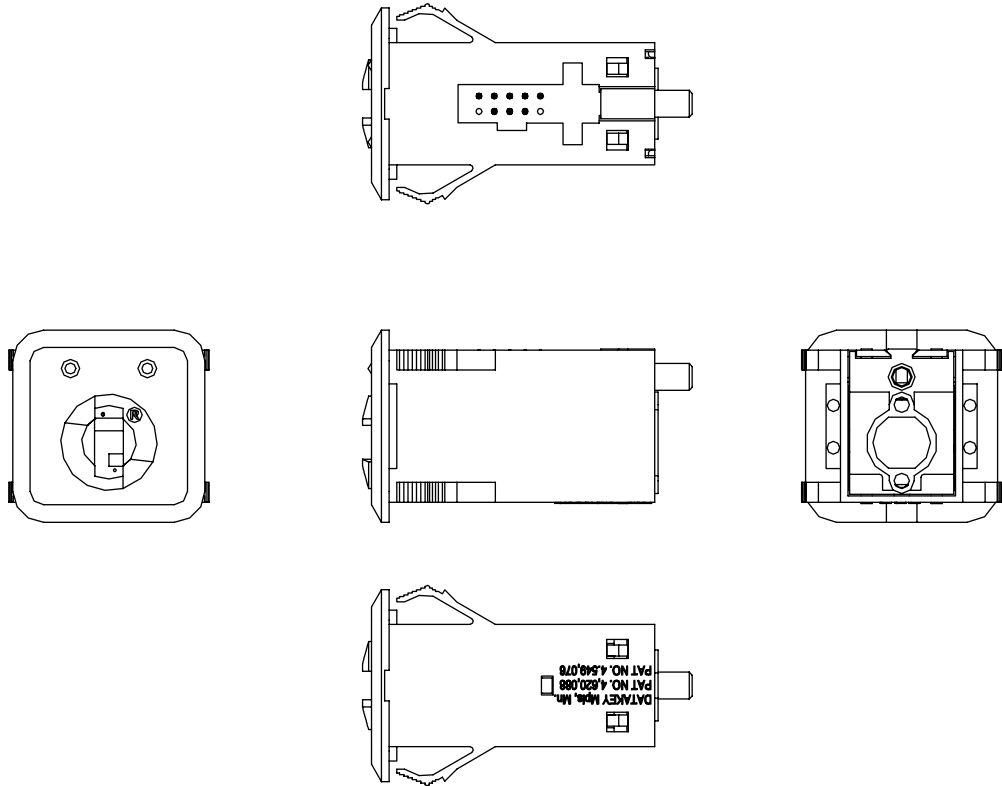
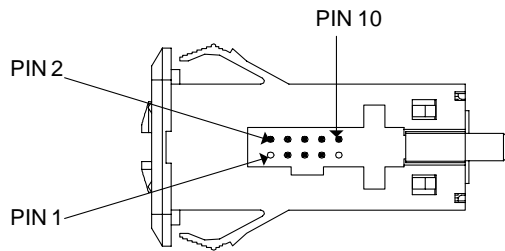


Figure 16: KC4210 Keyceptacle Orthographic Drawing

Continued on next page

Panel- and board-mount Keyceptacle[®]/Receptacle descriptions, continued

KC4210 pin outs Figure 17 shows KC4210 Keyceptacle pin outs.



Pin No.	Description
Pin 1	NC
Pin 2	Power (V_{CC})
Pin 3	Ground (V_{SS})
Pin 4	/HOLD
Pin 5	Chip Select (/CS)
Pin 6	Serial Data In (SI)
Pin 7	Serial Clock (SCK)
Pin 8	Serial Data Out (SO)
Pin 9	NC
Pin 10	LOFO

Keyceptacle
Bottom View

Figure 17: KC4210 Keyceptacle Pin Outs

Continued on next page

Panel- and board-mount Keyceptacle®/Receptacle descriptions, continued

KC4210PCB board-mount Keyceptacle

The KC4210PCB board-mount Keyceptacle is designed for applications where the designer wants to mount the device directly onto a printed circuit board (PCB). Figure 18 shows the KC4210PCB Keyceptacle. In these applications, the Keyceptacle connects to the host by soldering the leads onto a PCB.



Figure 18: KC4210PCB Board-Mount Keyceptacle

KC4210PCB orthographic drawing

Figure 19 shows the KC4210PCB Keyceptacle. Refer to spec sheet for dimensions.

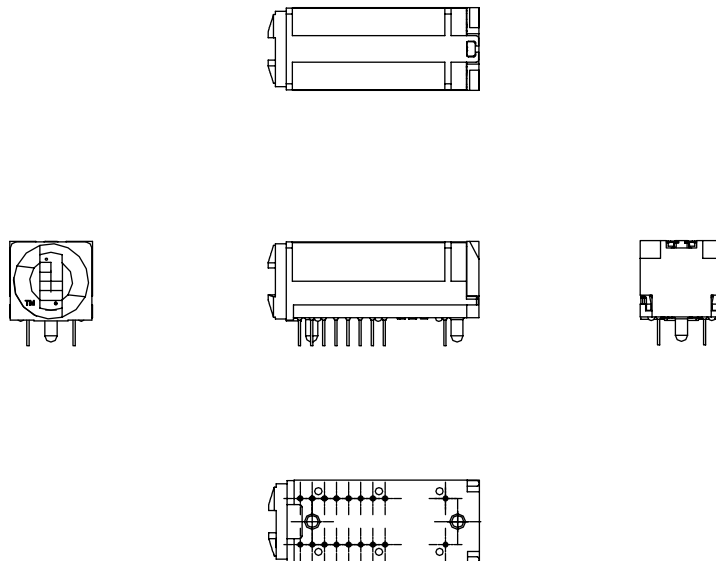
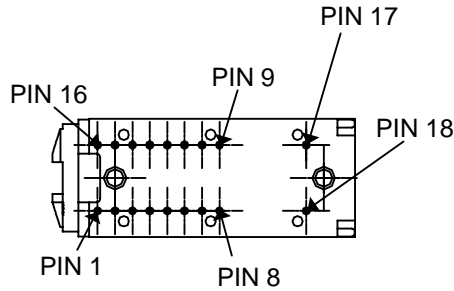


Figure 19: KC4210PCB Keyceptacle Orthographic Drawing

Continued on next page

Panel- and board-mount Keyceptacle®/Receptacle descriptions, continued

KC4210PCB pin outs Figure 20 shows KC4210PCB Keyceptacle pin outs.



Pin No.	Description
Pin 1	/HOLD
Pin 2	Ground (V_{SS})
Pin 3	Power (V_{CC})
Pin 4	NC
Pin 5	Serial Data Out (SO)
Pin 6	Chip Select (/CS)
Pin 7	Serial Clock (SCK)
Pin 8	Serial Data In (SI)
Pin 9	Serial Data In (SI)
Pin 10	Serial Clock (SCK)
Pin 11	Chip Select (/CS)
Pin 12	Serial Data Out (SO)
Pin 13	NC
Pin 14	Power (V_{CC})
Pin 15	Ground (V_{SS})
Pin 16	/HOLD
Pin 17	LOFO
Pin 18	LOFO

Figure 20: KC4210PCB Keyceptacle Pin Outs

KC4210 Key style The KC4210 panel- and board-mount Keyceptacles accept SFK and SFK5V Keys. See Figure 21.

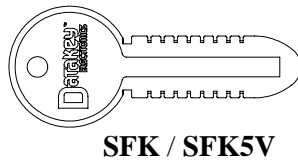


Figure 21: SFK and SFK5V Key

Continued on next page

Panel- and board-mount Keyceptacle®/Receptacle descriptions, continued

SR4210 panel-mount Receptacle

The SR4210 panel-mount version is designed for applications that require easy mounting in a front-panel configuration. To mount the SR4210 panel-mount Receptacle, simply cut a hole based on the dimensions shown on the SR4210 spec sheet in the desired panel location and then slip it into place. A standard 10-pin connector cable (5 x 2) is used to connect the device to the host. A Last On/First Off (LOFO) switch in the Receptacle enables the host system to determine when a Token is present. Figure 22 shows the SR4210 panel-mount Receptacle.



Figure 22: SR4210 Panel-Mount Receptacle and Clip

Note: Do not allow the total length of the signal conductors for PC board traces and ribbon cables to exceed eight inches.

SR4210 orthographic drawing

Figure 23 shows the SR4210 panel-mount Receptacle. Refer to spec sheet for dimensions.

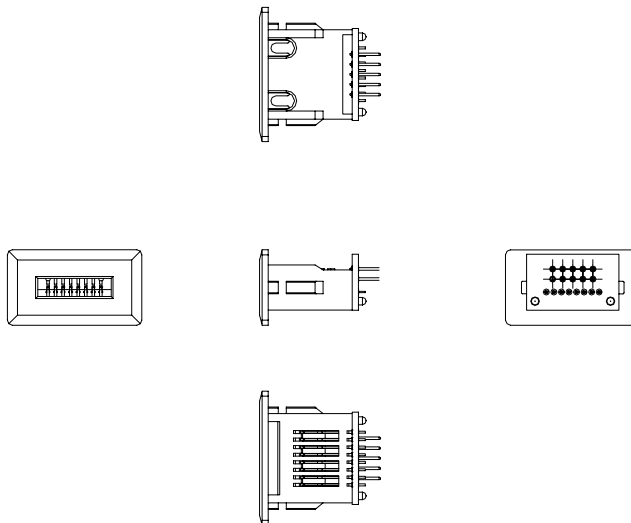


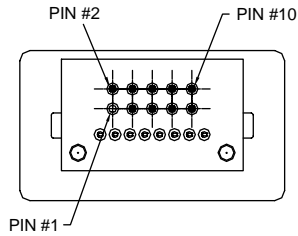
Figure 23: SR4210 Receptacle Orthographic Drawing

Continued on next page

Panel- and board-mount Keyceptacle®/Receptacle descriptions, continued

SR4210 pin outs

Figure 24 shows SR4210 panel-mount Receptacle pin outs.



Pin	Description
Pin 1	NC
Pin 2	Power (V_{CC})
Pin 3	Ground (V_{SS})
Pin 4	NC
Pin 5	Chip Select ($/CS$)
Pin 6	Serial Data In (SI)
Pin 7	Serial Clock (SCK)
Pin 8	Serial Data Out (SO)
Pin 9	$/HOLD$
Pin 10	LOFO

Figure 24: SR4210 Receptacle Pin Outs

Continued on next page

Panel- and board-mount Keyceptacle®/Receptacle descriptions, continued

SR42XXPCB mount Receptacles

The information on the SR4210PCB below also applies to the SR4220, SR4230 board-mount Receptacles. Dimensions can be found in the corresponding spec sheets. Contact the factory for information on SMT options.

SR4210PCB board-mount receptacle

The SR4210PCB board-mount Receptacle is designed for applications where the designer wants to mount the device directly onto a printed circuit board (PCB). Figure 25 shows the SR4210PCB board-mount Receptacle. In these applications, the Receptacle connects to the host by soldering the leads onto a PCB.



Figure 25: SR4210PCB Board-Mount Receptacle

SR4210PCB orthographic drawing

Figure 26 shows the SR4210PCB board-mount Receptacle. Refer to spec sheet for dimensions.

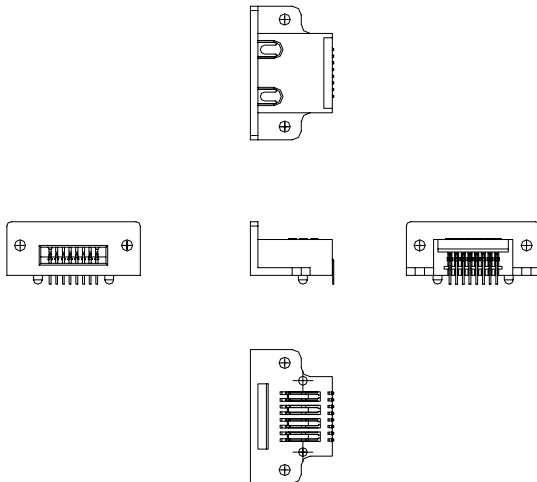


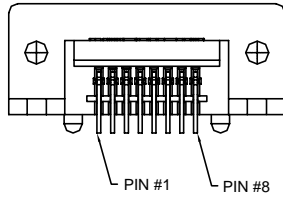
Figure 26: SR4210PCB Board-Mount Orthographic Drawing

Continued on next page

Panel- and board-mount Keyceptacle®/Receptacle descriptions, continued

SR4210PCB pin outs

Figure 27 shows SR4210PCB Receptacle pin outs.



Pin	Description
Pin 1	/HOLD
Pin 2	Power (Vcc)
Pin 3	Chip Select (/CS)
Pin 4	Serial Clock (SCK)
Pin 5	Serial Data In (SI)
Pin 6	Serial Data Out (SO)
Pin 7	Ground (Vss)
Pin 8	LOFO

Figure 27: SR4210PCB Pin Outs

Slim Token styles

The SR4210 panel- and PCB-mount Receptacles accept the IST- and ISX-Token style with memory sizes from 1Kb to 512Kb. Figure 28 shows the Token styles.

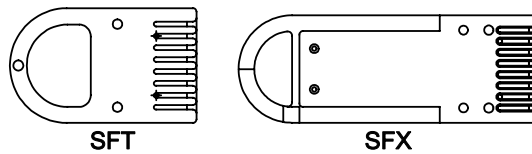


Figure 28: SFT Token and SFX Extended Token Styles

Electrical interface

SPI Flash Interface Specification

AC/DC electrical characteristics

Tables 5 thru 8 show specific common DC and AC electrical characteristics for SPI Flash Keys and Tokens. These devices are available with nominal supply voltages of 3.3 and 5.0 volts. Table 5 shows the absolute maximums for both versions of the Keys and Tokens. Table 6 shows the DC operating characteristics for the 3.3-volt version. Table 7 shows the DC operating characteristics for the 5.0-volt version. Table 8 shows the AC characteristics for the devices.

Maximum specifications

Stressing SPI Flash Keys and Tokens beyond the limits specified in Table 5 could cause permanent damage to the device. The conditions are stress ratings only. Exposure to absolute maximum stress levels for extended periods could affect device reliability. Tables 6 thru 8 specify operating levels for the devices.

Table 5: Absolute Maximum Values and Temperature

Symbol	Parameter	Min/Max	Units
V _{CC}	Supply Voltage (3.3 volt versions)	-0.6 to 4.0	V
	Supply Voltage (5.0 volt versions)	-0.3 to 6.0	V
V _{IN/OUT}	All pins w.r.t. Ground (3.3 volt versions)	-0.6 to 4.0	V
	All pins w.r.t. Ground (5.0 volt versions)	-0.3 to 6.0	V
T _{STG}	Storage temperature	-65 to 150	°C
T _{BIAS}	Operating temperature	-40 to 85	°C

Continued on next page

Table 6: DC Characteristics for 3.3-Volt Keys and Tokens

Symbol	Parameter	Min	Max	Units	Conditions
V _{CC}	Supply voltage	2.7	3.6	V	
V _{IH}	High-level voltage input	0.7V _{CC}	V _{CC} + 0.4	V	
V _{IL}	Low-level voltage input	-0.3	0.3V _{CC}	V	
V _{OH}	High-level voltage output	V _{CC} - 0.2		V	I _{OH} = -100 μA
V _{OL}	Low-level voltage output		0.4	V	I _{OL} = 1.6 mA
I _{LI}	Input leakage current		± 2	μA	
I _{LO}	Output leakage current		± 2	μA	
I _{CC1}	Standby current		50.0	μA	/CS = V _{CC} , V _{IN} = V _{CC} or V _{SS}
I _{CC2}	Deep power-down current		5.0	μA	/CS = V _{CC} , V _{IN} = V _{CC} or V _{SS}
I _{CC3}	Operating current (<i>read</i>)		15.0	mA	SCK = 0.1V _{CC} to 0.9V _{CC} , 25MHz, SO = open
I _{CC4}	Operating current (<i>page program</i>)		20.0	mA	/CS = V _{CC}
I _{CC5}	Operating current (<i>write status reg</i>)		20.0	mA	/CS = V _{CC}
I _{CC6}	Operating current (<i>sector erase</i>)		25.0	mA	/CS = V _{CC}
I _{CC7}	Operating current (<i>chip erase</i>)		25.0	mA	/CS = V _{CC}
C _{OUT}	Output capacitance		8.0	pF	V _{OUT} = 0
C _{IN}	Input capacitance		6.0	pF	V _{IN} = 0

Continued on next page

Electrical interface, continued

Table 7: DC Electrical Characteristics for 5.0-Volt Keys and Tokens

Symbol	Parameter	Min	Max	Units	Conditions
V _{CC}	Supply voltage	3.8	5.5	V	
V _{IH}	High level voltage input	V _{CC} - 0.4	V _{CC}	V	
V _{IL}	Low level voltage input	0.0	0.2	V	
V _{OH}	High level voltage output	0.67V _{CC}		V	I _{OH} = -100 μ A
V _{OL}	Low level voltage output		0.4	V	I _{OL} = 1.6 mA
I _{CC1}	Standby current		1.0	mA	/CS = V _{CC} , V _{IN} = V _{CC} or V _{SS}
I _{CC2}	Deep power-down current		1.0	mA	/CS = V _{CC} , V _{IN} = V _{CC} or V _{SS}
I _{CC3}	Operating current (<i>read</i>)		16.0	mA	SCK = 0.1V _{CC} to 0.9V _{CC} , 25MHz, SO = open
I _{CC4}	Operating current (<i>page program</i>)		21.0	mA	/CS = V _{CC}
I _{CC5}	Operating current (<i>write status reg</i>)		21.0	mA	/CS = V _{CC}
I _{CC6}	Operating current (<i>sector erase</i>)		26.0	mA	/CS = V _{CC}
I _{CC7}	Operating current (<i>chip erase</i>)		26.0	mA	/CS = V _{CC}

Continued on next page

Table 8: AC Characteristics

Symbol	Parameter	Min	Max	Units	Notes
F _{SCK}	SCK Clock Frequency	D.C.	25	MHz	(see note 1)
F _{SCKR}	SCK Clock Frequency for Read	D.C.	20	MHz	(see note 1)
t _{SRT}	Clock rise time	0.1		V/ns	
t _{SRF}	Clock fall time	0.1		V/ns	
t _{SH}	Clock high time	18		ns	(see notes 2, 3)
t _{SL}	Clock low time	18		ns	(see notes 2, 3)
t _{CSD}	Chip select deselect time (relative to clock)	100		ns	
t _{CSS}	Chip select setup time (relative to clock)	10		ns	
t _{CSH}	Chip select hold time (relative to clock)	10		ns	
t _{DSU}	Data In setup time	5		ns	
t _{DH}	Data In hold time	5		ns	
t _V	Clock low to data valid		15	ns	
t _{HO}	Output hold time	0		ns	
t _{HLSH}	/Hold setup time (relative to clock)	10		ns	
t _{SHHH}	/Hold hold time (relative to clock)	10		ns	
t _{HHS}	Hold setup time (relative to clock)	10		ns	
t _{SHHL}	Hold hold time (relative to clock)	10		ns	
t _{LZ}	Hold to output low-Z		15	ns	
t _{HZ}	/Hold to output high-Z		20	ns	
t _{DIS}	Output disable time		15	ns	
t _{DP}	/CS high to power down mode		3	μs	
t _W	Write status register write time		15	ms	
t _{PP}	Page Program cycle time (256 bytes)		10	ms	
t _{SE}	Sector Erase cycle time		3	s	
t _{BE}	Bulk Erase cycle time, 1 Mbit		6	s	
t _{BE}	Bulk Erase cycle time, 2 Mbit		6	s	
t _{BE}	Bulk Erase cycle time, 4 Mbit		10	s	
t _{BE}	Bulk Erase cycle time, 8 Mbit		20	s	

Continued on next page

Electrical interface, continued

Notes:

1. Due to level shifting circuitry, the maximum clock frequency for 5-volt Keys and Tokens is limited to 8MHz for "push-pull" driving configurations and 500 KHz for "open-drain" driving configurations.
 2. $t_{SH} + t_{SL}$ must be greater than or equal to $1/f_{SCK}$.
 3. Minimum times for t_{SH} and t_{SL} are 250 ns ("push-pull" configuration) and 4000 ns ("open-drain" configuration) for 5-volt Keys and Tokens while in operation.
-

Timing diagrams

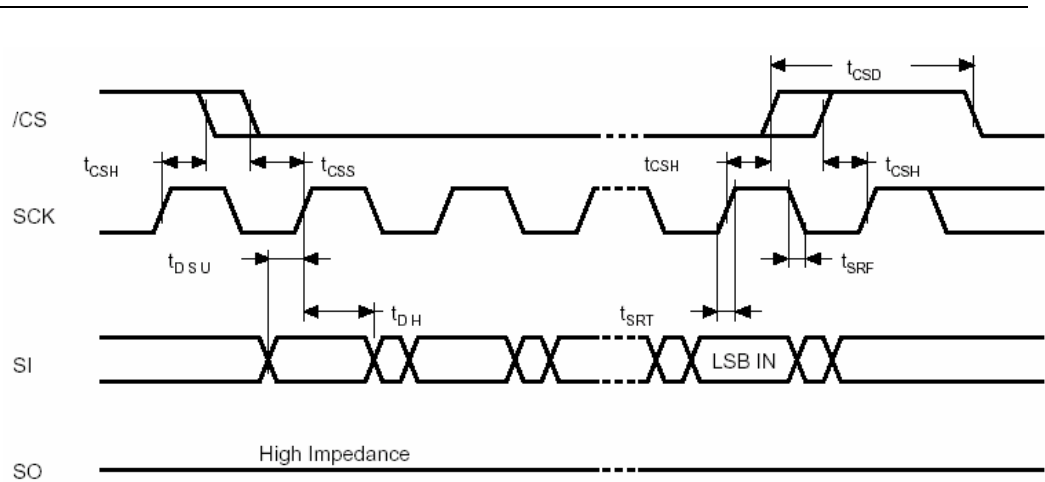


Figure 29: Serial Input Timing

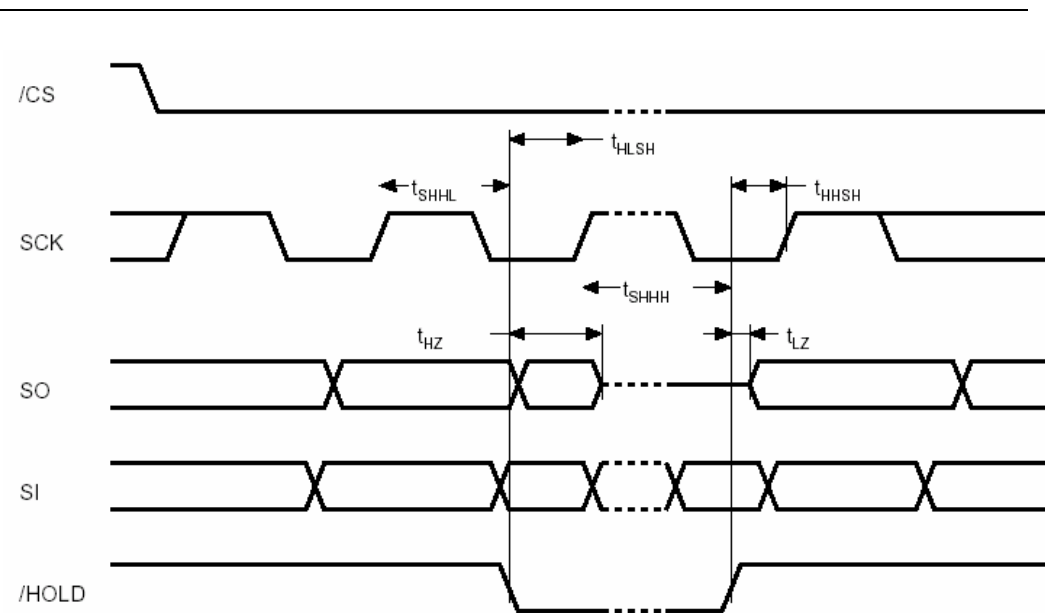


Figure 30: Hold Timing

Continued on next page

Timing diagrams, continued

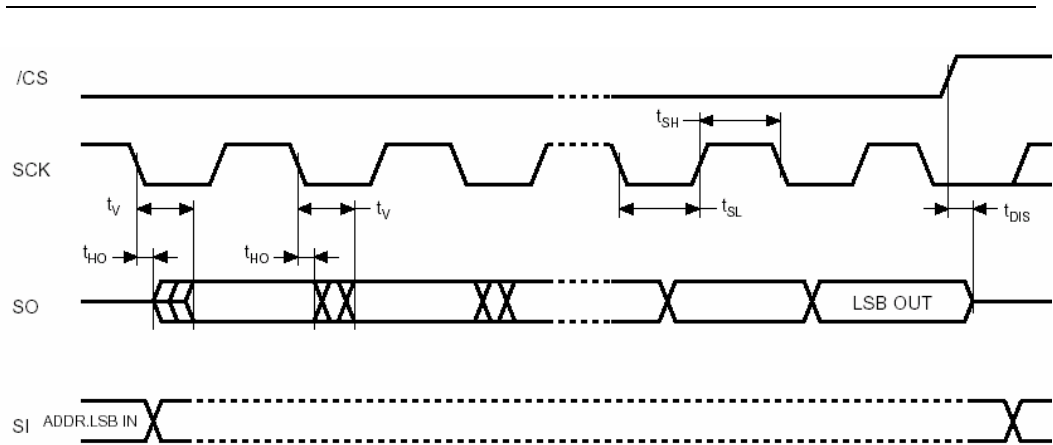


Figure 31: Output Timing



Electrostatic discharge (ESD)

Circuit component damage

A buildup of electrostatic charge gradients across the surface of a memory device can produce voltages that could damage circuit components. To prevent this damage, Datakey Electronics portable memory devices integrate materials, circuits, and mechanical barriers that help to ensure uniform voltages across the circuit.

Electrostatic charge voltage levels

Any system that uses memory devices must also provide a means of dissipating electrostatic charges. By simply holding a portable memory device in your hand, it is possible to build up an electrostatic charge across the surface of the memory device up to 20KV relative to ground. This would be equivalent to connecting a circuit of several hundred picofarads of capacitance with a low-series resistance to the memory device.

Electrostatic charge dissipation

When inserting a Key or Token into a grounded system or at some other potential, there must be a way to dissipate the built-up charge on the device from handling. You can do this by providing a path to ground for the charge. To prevent high-current and high-voltage buildups in the device and system, place a resistor in the circuit trace of the system. Then use over-voltage protection devices to direct the charge to system ground.

Memory device power and signal control

Poor contact concerns

When inserting a portable memory device into a host system, there can be poor contact between the memory device and the host system. There can be several possible reasons for this:

- **Dirty contact surfaces:** To make enough electrical contact, the contact surfaces must be free of contaminants. This requires cleaning the contacts through a wiping action from the portable memory device.
 - The contacts could bounce and require some time to settle. This could result in a series of random make and break conditions on any or all of the contacts.
 - When removing a memory device from a host system, the contacts might not always break evenly or cleanly.
-

Power concerns

Applying power to a memory device as you insert or remove it from a host system could cause random contact makes and breaks, causing significant problems for the memory device and the host. This happens because the control and address signals are not controlled during those actions. Therefore, undesirable logic combinations could occur, such as the following:

- Power and ground connections that become unstable can cause further unpredictability.
 - Fast-power switching to a memory device introducing noise into system power and ground distribution circuits could result in electrical damage to the memory device and corruption to its data.
-

Data corruption concerns

The integrated circuits used in Datakey Electronics memory devices are designed to reduce the risk of data corruption during transient conditions. For example, memory devices require a Write Enable instruction before storing any data. Write instructions will not execute if the supply voltage is less than a predetermined value. As effective as these protection schemes might be, however, they do not always eliminate the potential problems with noise that might occur when power is applied to a circuit via a bouncing contact.

To avoid these problems, it is important to control the memory-device power and signal connections. This can be done by using detection circuits, which are discussed next.

Continued on next page

Memory device power and signal control, continued

Memory device detection circuit The memory device detection circuit senses when a memory device is present. Datakey Electronics Keyceptacles[®]/Receptacles use Last On/First Off (LOFO) contacts for this purpose. When inserting a memory device into the Keyceptacle/Receptacle, the LOFO contacts make electrical connection only after closing all other contacts. Similarly, the LOFO contacts break before any other contact is open.

Transistor switch circuit When a Receptacle detects a memory device for a certain minimum time, power can then be applied. You can control the application of power by using a simple transistor switch circuit that meets the following conditions:

- The power switch should have a low voltage drop when power is applied to the memory device. This ensures that the supply voltage to the memory device is within its tolerance.
- The circuit should apply power to any pull-up resistors connected to the memory device to prevent power from being applied unintentionally through the signal lines.
- The circuit should include a bleeder resistor to ensure that power is removed quickly when the switch is turned OFF.
- The switch should turn power ON fast enough to avoid causing problems in the memory device and slow enough so that it does not introduce any significant noise into the system-reset circuit.

SPI Flash read and write procedures

Procedures Follow the procedures below when using a portable memory device in a host system with a power-switching circuit.

Read procedure The procedure for reading data from a memory device is less critical than the sequence for writing data to that same device because the data is not subject to change. To read the data from a memory device, Datakey Electronics recommends the following procedure:

Insert the memory device

Detect a memory device using the LOFO contact

Wait for the contacts to settle (verify that the memory device is still present)

Apply power

Wait for power to stabilize

Test contact integrity

Read data

Remove power

Remove the memory device

Continued on next page

SPI Flash read and write procedures, continued

Write procedure

The write procedure must verify that the memory device is present throughout the write cycle; this will ensure that data is written to the memory device correctly. To write data to a memory device, Datakey Electronics recommends the following procedure:

Insert the memory device

Detect a memory device using the LOFO contact

Wait for contacts to settle (verify that the memory device is still present)

Apply power

Wait for power to stabilize

Test contact integrity

Write data

Verify that the memory device is still present (*if not, indicate an error*)

Verify the written data (if appropriate, indicate an error)

Remove power

Remove the memory device

Long read/write operations

Large capacity memory systems should also be protected against memory device removal during a long read or write operation. An activity light could be all that is needed for some applications. Other installations could require physical barriers or interlocks to ensure that the memory device being read or written to remains in place.

Addendum A (Sizes Greater than 8Mbits)

The following tables provide information regarding the memory organization and block protection for the SFK32M Keys and SFX32M/SFX64M Tokens.

All commands described in the SPI Flash Interface Specification apply to the SFK32M and SFX32M/SFX64M. All electrical interface information provided in tables 5, 6, and 8 apply to the 32M/64M products. The bulk erase time (t_{BE}) for the 32M products is a maximum of 80 seconds. The bulk erase time (t_{BE}) for the 64M products is a maximum of 160 seconds.

Block Protect Bit Settings

Block Protect Bits			SFK 32M SFX 32M	SFX 64M
BP2	BP1	BP0	Protected Sectors	
0	0	0	None	None
0	0	1	63	126 and 127
0	1	0	62 and 63	124 to 127
0	1	1	60 to 63	120 to 127
1	0	0	56 to 63	112 to 127
1	0	1	48 to 63	96 to 127
1	1	0	32 to 63	64 to 127
1	1	1	All	All

Continued on next page



Memory Organization Table

	SFK 32M SFX 32M		SFX 64M
Device Signature	15h		16h
Device Size (Bytes)	4194304		8388608
Pages	16384		32768
Page Size (Bytes)	256		256
Sectors	64		128
Sector Size (Bytes)	65536		65536
Sector	Address Range	Sector	Address Range
0	000000h to 00FFFFh	32	200000h to 20FFFFh
1	010000h to 01FFFFh	33	210000h to 21FFFFh
2	020000h to 02FFFFh	34	220000h to 22FFFFh
3	030000h to 03FFFFh	35	230000h to 23FFFFh
4	040000h to 04FFFFh	36	240000h to 24FFFFh
5	050000h to 05FFFFh	37	250000h to 25FFFFh
6	060000h to 06FFFFh	38	260000h to 26FFFFh
7	070000h to 07FFFFh	39	270000h to 27FFFFh
8	080000h to 08FFFFh	40	280000h to 28FFFFh
9	090000h to 09FFFFh	41	290000h to 29FFFFh
10	0A0000h to 0AFFFFh	42	2A0000h to 2AFFFFh
11	0B0000h to 0BFFFFh	43	2B0000h to 2BFFFFh
12	0C0000h to 0CFFFFh	44	2C0000h to 2CFFFFh
13	0D0000h to 0DFFFFh	45	2D0000h to 2DFFFFh
14	0E0000h to 0EFFFFh	46	2E0000h to 2EFFFFh
15	0F0000h to 0FFFFFh	47	2F0000h to 2FFFFFh
16	100000h to 10FFFFh	48	300000h to 30FFFFh
17	110000h to 11FFFFh	49	310000h to 31FFFFh
18	120000h to 12FFFFh	50	320000h to 32FFFFh
19	130000h to 13FFFFh	51	330000h to 33FFFFh
20	140000h to 14FFFFh	52	340000h to 34FFFFh
21	150000h to 15FFFFh	53	350000h to 35FFFFh
22	160000h to 16FFFFh	54	360000h to 36FFFFh
23	170000h to 17FFFFh	55	370000h to 37FFFFh
24	180000h to 18FFFFh	56	380000h to 38FFFFh
25	190000h to 19FFFFh	57	390000h to 39FFFFh
26	1A0000h to 1AFFFFh	58	3A0000h to 3AFFFFh
27	1B0000h to 1BFFFFh	59	3B0000h to 3BFFFFh
28	1C0000h to 1CFFFFh	60	3C0000h to 3CFFFFh
29	1D0000h to 1DFFFFh	61	3D0000h to 3DFFFFh
30	1E0000h to 1EFFFFh	62	3E0000h to 3EFFFFh
31	1F0000h to 1FFFFFh	63	3F0000h to 3FFFFFh

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Memory Organization Table (continued)

Sector	Address Range	Sector	Address Range
64	400000h to 40FFFFh	96	600000h to 60FFFFh
65	410000h to 41FFFFh	97	610000h to 61FFFFh
66	420000h to 42FFFFh	98	620000h to 62FFFFh
67	430000h to 43FFFFh	99	630000h to 63FFFFh
68	440000h to 44FFFFh	100	640000h to 64FFFFh
69	450000h to 45FFFFh	101	650000h to 65FFFFh
70	460000h to 46FFFFh	102	660000h to 66FFFFh
71	470000h to 47FFFFh	103	670000h to 67FFFFh
72	480000h to 48FFFFh	104	680000h to 68FFFFh
73	490000h to 49FFFFh	105	690000h to 69FFFFh
74	4A0000h to 4AFFFFh	106	6A0000h to 6AFFFFh
75	4B0000h to 4BFFFFh	107	6B0000h to 6BFFFFh
76	4C0000h to 4CFFFFh	108	6C0000h to 6CFFFFh
77	4D0000h to 4DFFFFh	109	6D0000h to 6DFFFFh
78	4E0000h to 4EFFFFh	110	6E0000h to 6EFFFFh
79	4F0000h to 4FFFFFFh	111	6F0000h to 6FFFFFFh
80	500000h to 50FFFFh	112	700000h to 70FFFFh
81	510000h to 51FFFFh	113	710000h to 71FFFFh
82	520000h to 52FFFFh	114	720000h to 72FFFFh
83	530000h to 53FFFFh	115	730000h to 73FFFFh
84	540000h to 54FFFFh	116	740000h to 74FFFFh
85	550000h to 55FFFFh	117	750000h to 75FFFFh
86	560000h to 56FFFFh	118	760000h to 76FFFFh
87	570000h to 57FFFFh	119	770000h to 77FFFFh
88	580000h to 58FFFFh	120	780000h to 78FFFFh
89	590000h to 59FFFFh	121	790000h to 79FFFFh
90	5A0000h to 5AFFFFh	122	7A0000h to 7AFFFFh
91	5B0000h to 5BFFFFh	123	7B0000h to 7BFFFFh
92	5C0000h to 5CFFFFh	124	7C0000h to 7CFFFFh
93	5D0000h to 5DFFFFh	125	7D0000h to 7DFFFFh
94	5E0000h to 5EFFFFh	126	7E0000h to 7EFFFFh
95	5F0000h to 5FFFFFFh	127	7F0000h to 7FFFFFFh

Acknowledgement

ST Microelectronics Timing diagrams are the courtesy of ST Microelectronics, and are reprinted by permission.

Revision history

Date	Revision	Description
2/21/2005	A	Initial issue of SPI Flash interface specification.
3/28/05	B	Reformatted to new template.
8/31/06	C	Add Addendum A, corrections
9/20/07	D	Removed dimensions from drawings; updated Addendum A for 64Mbit devices; updated for corporate identity
11/29/07	E	Clarify SR4210PCB pin out to entire SR4000 Receptacle family.

SPI Flash Interface Specification



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